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10/709,823	06/01/2004	Che-Hui Chang Chien	13353-US-PA	3822

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
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EXAMINER	
NGUYEN, TANH Q	
ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,823	CHANG CHIEN ET AL.	
	Examiner	Art Unit	
	TANH Q. NGUYEN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The amendment filed September 25, 2008 is objected to because there is no evidence that the original disclosure supports the data output latch 415 **determining** to output the nonreal-time data via the data output bus according to the control of the control unit 411 (see amendment to [0029], lines 8-12).

In the Remarks, applicant essentially indicates that "*Since it is obvious that from FIG. 4 and general available knowledge from one of ordinary skill in the art, the non-real time data latched in the data output latch 415 must be output*" supports "the data output latch 415 determining to output the nonreal-time data via the data output bus according to the control of the control unit 411.

While the latched nonreal-time data must be output in accordance with control of the control logic unit 411, it is **not obvious** from FIG. 4 and general available knowledge from one of ordinary skill in the art that the data output latch 415 **determines** to output the nonreal-time data via the data output bus according to the control of the control unit 411.

It is only **obvious** from FIG. 4 and general available knowledge from one of ordinary skill in the art that the data output latch 415 outputs the nonreal-time data via the data output bus according to the control of the control unit 411.

Applicant is required to amend the specification accordingly in the reply to this Office Action.

Claim Objections

2. Claims 1-3, 8 are objected to because of the following informalities:

Claim 1 recites "the control logic unit controls the data output latch to latch the nonreal-time data, and **determines** to output the nonreal-time data from the data output latch" in lines 22-24. FIG.4 and general available knowledge from one of ordinary skill in the art appear to support only "the control logic unit controls the data output latch to latch the nonreal-time data and to output the nonreal-time data". Appropriate correction is required.

“a flag register coupled to the buffer for storing a flag indicating a state of the buffer” in the last 2 lines of claim 2 should be replaced with --a flag register coupled to the buffer for storing a flag state--to be consistent with the specification ([0027], lines 16-17).

“wherein when the flag indicating the state of the 3-state buffer in the flag register is setting/reading, the 3-state buffer is in an “on” state, and wherein when the flag indicating the state of the 3-state buffer in the flag register is not setting/reading, the 3-state buffer is in a high impedance state” in lines 2-6 of claim 3 should be replaced with --wherein when the flag state in the flag register is being set/read, the 3-state buffer is in an “on” state, and wherein when the flag state in the flag register is not being set/read, the 3-state buffer is in a high impedance state—to be consistent with the specification ([0028], lines 1-6).

"to convert a type of the real-time data from TTL to differential or from differential to TTL" in lines 4-5 in claim 8 should be replaced with --to convert the real-time data

from TTL to differential, or from differential to TTL-- for clarity.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sparr et al. (US 2002/0176390 A1) in view of Hirairi (US 6,480,942)/Rangan et al. (US RE39,395), and further in view of Hao et al. (US 6,760,873) /Feda (US 2004/0247080).

5. As per claim 1, Sparr teaches a real-time data transmission interface [246,235 - FIG. 4] coupled between a real-time system for providing real-time data [[0063], lines 5-7] and a host computer [245, FIG. 4] for providing nonreal-time data [[0063], line 1], the real-time data transmission interface being suitable for transmitting the nonreal-time data [290, FIG. 5] in real-time from the host computer to the real-time system [294, FIG. 5], and for transmitting the real-time data [293, FIG. 5] in nonreal-time from the real-time system to the host computer [289, FIG. 5], the real-time data transmission interface comprising:

a nonreal-time data interface unit [251,258 - FIG. 5] for receiving/transmitting the nonreal-time data;

a memory unit [295, FIG. 5] for caching the nonreal-time data [292, FIG. 5] and the real-time data [291, FIG. 5]; and

a network interface control unit [293, 294 - FIG. 5; 235, 273 - FIG. 4] coupled to the memory unit for receiving/transmitting the real-time data.

Sparr does not teach the real-time system being a radar system.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the real-time data transmission interface of Sparr with a radar system being a real-time system because a radar system is no more than a system of a set of real-time systems, and because the use of a radar system with the real-time data transmission interface of Sparr would yield the predictable results of the real-time data transmission interface being suitable for transmitting nonreal-time data from the host computer to the radar system and transmitting the real-time data in nonreal-time from the radar system to the host computer. *See KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (2007).*

It would have been also obvious to one of ordinary skill in the art at the time the invention was made to use the real-time data transmission interface of Sparr with a radar system instead of the real-time system of Sparr because the substitution of a the real-time system of Sparr with a radar system would yield the predictable results of the real-time data transmission interface being suitable for transmitting nonreal-time data from the host computer to the radar system and transmitting the real-time data in nonreal-time from the radar system to the host computer. See KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (2007).

It would have been also obvious to one of ordinary skill in the art at the time the invention was made to use the real-time data transmission interface of Sparr with a

radar system instead of the real-time system of Sparr because the substitution of the real-time system of Sparr with a radar system are within the ordinary capabilities of one of ordinary skill in the art. *See KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (2007).*

Furthermore, since the real-time system of Sparr is a system of a set of real-time systems and since a radar system is another system of the set of real-time systems, the radar system is therefore no more than an obvious variant of the real-time system of Sparr. It would have been also obvious to one of ordinary skill in the art at the time the invention was made to use the real-time data transmission interface of Sparr with a radar system instead of the real-time system of Sparr because the radar system is no more than an obvious variant of the real-time system of Sparr.

Furthermore, since applicant discloses a radar system being an example of a real-time signal processing apparatus [page 2, [0005], lines 5-6], and since applicant does not indicate the radar system being critical to the invention, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the use of a radar system in applicant's disclosure is application specific. Patentability cannot be accorded to an invention merely because it is directed to a specific application.

Sparr essentially does not teach an I/O unit that is coupled to the nonreal-time data interface unit; the I/O unit being used as a transmission interface for the nonreal-time data and the real-time data; wherein the memory unit is coupled to the I/O unit and wherein the I/O unit further includes a control logic, a checking circuit, a data output latch and a data input latch – as recited in lines 17-26 of the claim.

Hirairi teaches a FIFO (21, FIG. 8A) with an input register (31, FIG. 8A) coupled to a control logic (11-1, FIG. 8A) for receiving data prior to transferring to the FIFO – hence suggests an I/O unit comprising a data output latch coupled to the control logic unit. Hirairi also teaches a FIFO (21, FIG. 8A) with an output register (32, FIG. 8A) coupled to a control logic (11-1, FIG. 8A) for receiving data transferred from the FIFO - hence suggests an I/O unit comprising a data input latch coupled to the control logic unit.

Hirairi further teaches using an input register when a considerable amount of time is required to read from the FIFO, and using an output register when a considerable amount of time is required to write to the FIFO (col. 2, line 66-col. 3, line 7). Hirairi's teachings, when incorporated with the memory unit of Sparr would result in the memory unit of Sparr being coupled to an I/O unit, the I/O unit being coupled to the nonreal-time data interface unit and being used as a transmission interface for the nonreal-time data and the real-time data. Rangan teaches the data writing into a FIFO (1432, FIG. 14) being more robust when data is loaded into a latch (1416a, FIG. 14; col. 20, lines 55-61) - hence also suggests the data reading from the FIFO being more robust when data is loaded into a latch from the FIFO

It would have been obvious to one of ordinary skilled in the art to incorporate the teachings of Hirairi in Sparr when a considerable amount of time is required to read from the memory and when a considerable amount of time is required – as is suggested by Harairi, or when data writing into the memory and data reading from the memory need to be more robust – as is suggested by Rangan.

The combination of Sparr with Harairi would therefore result in an I/O unit comprising:

a control logic unit for controlling the I/O unit to perform an input/output operation according to an external control signal (a logic component 11-1 of Harairi for controlling an input operation of the I/O unit according to a WRITE ENABLE, and a logic component 11-1 of Harairi for controlling an output operation of the I/O unit according to a READ ENABLE – FIG. 8A of Harairi)

a data output latch (31, FIG. 8A of Harairi) coupled to the control logic unit, wherein when the nonreal-time data is transmitted via the I/O unit, the control logic unit controls the data output latch to latch the nonreal-time data and output the nonreal-time data to the memory unit (memory component 292, FIG. 5 of Sparr); and

a data input latch (32, FIG. 8A of Harairi) coupled to the control logic unit, wherein when the real-time data is read via the I/O unit, the data input latch receives the real-time data from the memory unit (memory component 291, FIG. 5 of Sparr).

Harairi does not teach a checking circuit coupled to the control logic unit - wherein when a self test mode is activated, the control logic unit controls the checking circuit to check an accuracy of data output from the I/O unit and generate a checking result.

Hao teaches checking circuit (a self test logic: col. 2, lines 54-60) coupled to a control logic unit (160, FIG. 3B) - wherein when a self test mode is activated, the control logic unit controls the checking circuit to check an accuracy of data output from the I/O unit and generate a checking result (a self test logic configured to test the accuracy of

the data for an input/output unit and generate an output signal: col. 2, lines 54-60). Feda teaches a self test means being provided for an I/O unit to achieve high data accuracy and generate an output signal ([0083]-[0084]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a checking unit, as is suggested by Hao/Feda in order to check an accuracy of data output from the I/O unit and to generate a checking result.

6. As per claims 6-7, Sparr/Harairi teaches the memory unit comprising:

a memory control logic unit for controlling the memory unit according to another external control signal (a memory control unit 22, FIG. 8A of Harairi for controlling memory component 292 of Sparr according to a WE signal, FIG. 8A of Harairi; and a memory control unit 22, FIG. 8A of Harairi for controlling memory component 291 of Sparr according to a RE signal, FIG. 8A of Harairi);

a first address counter (12, FIG. 7A of Harairi) coupled to the memory control logic unit for providing a first address;

a first memory (292, FIG. 5 of Sparr) coupled to the first address counter for storing the nonreal-time data;

a first buffer latch unit (32, FIG. 8A of Harairi) coupled to the first memory via an internal bus for working as an input/output interface of the first memory;

a second address counter (13, FIG. 7A of Harairi) coupled to the memory control logic unit for providing a second address;

a second memory (291, FIG. 5 of Sparr) coupled to the second address counter

for storing the real-time data; and

a second buffer latch unit (31, FIG. 8A of Harairi) coupled to the second memory via the internal data bus for working as an input/output interface of the second memory.

Harairi further teaches the memory unit comprising a flag register for storing a flag indicating a state of the memory unit (flag register 14, FIG. 7A for storing state of memory component 292 of Sparr, and flag register 14, FIG. 7A for storing state of memory component 291 of Sparr)

7. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sparr et al. in view of Hirairi/Rangan et al., Hao et al./Feda and further in view of Mano (Computer System Architecture) and Nishimukai et al. (US 6,381,680).

8. As per claims 2-3, Mano teaches a nonreal-time data interface unit (FIG. 11-2) comprising:

a bus interface unit (Bus buffers) working as an interface for inputting/outputting the nonreal-time data (via a bidirectional data bus);

a data output latch (Port A register or Port B register: last 3 lines on page 389) coupled to the bus interface unit via a first internal bus (Internal bus), wherein the data output latch is a latch for latching a data transmitted by the nonreal-time data interface unit to other units;

a data input latch (Port B register or Port A register: last 3 lines on page 389) coupled to the bus interface unit via the first internal bus, wherein the data input latch is a latch for latching a data transmitted by the other units and received by the nonreal-time data interface unit;

a control signal latch (Control register) coupled to the bus interface unit via the first internal bus, wherein the control signal latch is a latch for latching a control signal transmitted from the nonreal-time data interface unit to other units; and

a flag register (Status register) for storing a flag state.

Mano does not teach a buffer coupled to the bus interface unit via the first internal bus and the flag register being coupled to the buffer.

Nishimukai teaches a 3-state buffer (68, FIG. 9) coupled to a first bus (132, FIG. 9) being in an "on" state when data is written to a flag register (67, FIG. 9; col. 12, lines 21-25) or when data is read from the flag register (67, FIG. 9; col. 12, lines 21-25) - hence suggests the 3-state buffer being in an “on” state (i.e. connected state) when setting/reading the flag register, and the 3-state buffer being in an implicit high impedance state (i.e. behaving like open circuit, or disconnected) when not setting/reading the flag register (Mano, page 100, first paragraph of Three-State Bus Buffers).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a 3-state buffer between the bus interface unit and the flag register (hence a buffer coupled to the bus interface unit via the first internal bus and the flag register being coupled to the buffer) in order have the bus interface unit and the flag register behaviorally connected when setting/reading the flag state in the flag register, and to have the bus interface unit and the flag register behaviorally disconnected when not setting/reading the flag state in the flag register.

9. As per claim 4, Mano does not teach the nonreal-time data interface unit further comprising a clock generator for generating and providing a clock signal with a frequency of 10 MHz to other units.

Since applicant indicates that clock generator 313 may be included in the nonreal-time data interface unit ([0028], lines 5-8), applicant essentially suggests that the clock generator being included in the nonreal-time data interface unit being not critical to the invention.

Since it was known in the art at the time the invention was made to include a clock generator in a system for generating a clock signal and providing the clock signal to units within a system to operate the system and/or synchronize data transfer in the system, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a clock generator for generating a clock signal and providing the clock signal to units of the real-time data transmission interface in order to operate the real-time data transmission interface and/or synchronize data transfer in the real-time data transmission interface, with the clock generator being included in the nonreal-time data interface unit being no more than an obvious variant of the clock generator being included elsewhere in the real-time data transmission interface (because applicant does not consider the location of the clock generator being critical to the invention). In addition, since applicant does not indicate that a clock signal with a frequency of 10 MHz is critical to the invention, and since a frequency of 10 MHz is application and technology specific, no patentability can be accorded to an invention merely because it has an arbitrary value of 10 MHz or because it is directed to a specific

application or technology.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sparr et al. in view of Hirairi/Rangan et al., Hao et al./Feda and further in view of Christopher et al. (US 5,220,211) and Kosaraju (US 6,907,490).

Sparr teaches a network interface control unit (235, 273 – FIG. 4), but does not teach the network interface control unit comprising a programmable interface controller and a TTL/differential level converting interface, wherein the TTL/differential level converting interface is used to convert real- time data from TTL to differential or from differential to TTL.

Christopher teaches using a TTL/differential level converting interface [CV1, CV2 - FIG. 2] to convert data from TTL to differential, from differential to TTL - in order to minimize noise radiation [col. 6, lines 14-22; col. 6, lines 27-31; col. 6, lines 48-55]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a TTL/differential level converting interface, as is taught by Christopher, in order to minimize noise radiation.

Kosaraju teaches a network interface control unit (physical layer 212, FIG. 2; col. 3, lines 6-7; FIG. 6; FIG. 9) comprising a programmable interface controller (602, 654 - FIG. 6; 902, 924 - FIG. 9) for providing an interface between the network interface control unit and an I/O unit (210, FIG. 2; col. 3, lines 5-6; FIG. 7; FIG. 8) and for controlling routing within the network interface control unit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a programmable interface controller, as is taught by Kosaraju, in order to provide an

interface between the network interface control unit and the I/O unit and to control routing within the network interface control unit.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sparr et al. in view of Hirairi/Rangan et a., Hao et al. /Feda, Christopher et al./Kosaraju, and further in view of DeKoning et al. (US 6,385,683).

DeKoning teaches an interface controller comprising:

a sequencer (24, FIG. 1), coupled to a storage apparatus (14, 25 – FIG. 1) for adjusting a running order according to an external condition (col. 4, lines 42-44);

a condition selector (12, FIG. 1; col. 4, lines 39-40; col. 5, lines 13-14) coupled to the sequencer for generating the external condition;

an event/interrupt handler (24, 25 – FIG. 1; col. 4, lines 47-48; col. 4, line 61-col. 5, line 2) coupled to the storage apparatus for handling either an interrupt signal or an event;

a processor (12, FIG. 1) coupled to the storage apparatus for running microcode instructions; and

a parity generating/checking apparatus (26, FIG. 1; col. 4, lines 20-23) for either generating a parity bit according to data output from the interface controller or checking the parity bit of the data input into the programmable interface controller.

DeKoning teaches the above elements being used to carry out the functionalities of the interface controller. Furthermore, it was known in the art at the time the invention was made to store a microcode in a storage apparatus of an interface controller and use the microcode for controlling an operation of the interface controller. It would have been

obvious to one of ordinary skill in the art at the time the invention was made to store a microcode for controlling an operation of the interface controller in a storage apparatus of the interface controller in order to use the microcode to control the operation of the interface controller.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed elements in the programmable interface controller in order to carry out the functionalities of the programmable interface controller – as is suggested by DeKoning.

Response to Arguments

12. Applicant's arguments with respect to the pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TANH Q. NGUYEN whose telephone number is (571)272-4154. The examiner can normally be reached on M-F (9:30AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TARIQ HAFIZ can be reached on (571)272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TANH Q. NGUYEN/
Primary Examiner, Art Unit 2182

TQN: January 20, 2009